

## SIMPLE POWER DOWN CIRCUIT

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This circuit adds a power down function to analog I/O ports (for example, the AD7769 and AD7774). Moreover, the diodes ordinarily needed to protect the devices against power-supply missequencing can be eliminated. In the circuit, MOSFETs Q1 and Q2 switch the +5- and +12-V supplies, respectively, in a sequence controlled by two cross-coupled CD4001 CMOS NOR gates (U1C and U1D). The sequence in which power is applied is important: The controlled circuits may be damaged anytime  $V_{cc}$  exceeds  $V_{dd}+0.3V$ . Consequently, the NOR gates must be powered from a 12-V supply throughout the power-down sequence.

Bringing the power down control high (+5V) applies power to the controlled circuit by turning on all MOSFETs. Specifically, raising the power down brings the output of U1C low, causing capacitor C1 to discharge  $V_{OL}$  exponentially with time constant  $R1C1$ . As the voltage on C1 falls, two events occur. First, it puts a negative gate-source voltage on P-channel Q1, turning it on. Second, it causes output gate U1D to go high. With the output of U1D high, capacitor C2 charges exponentially to  $V_{OH}$ -about 12-V-applying a positive gate-source voltage to turn on Q2. In the power down mode, the Power Down control is brought low and the RC circuits and their delays work in reverse. Consequently, capacitor C2 discharges to the logic input of U1C before C1 can charge. Hence, Q2 turns off before Q1.